HYASiC
Digital Power ASIC

USB TYPE-C POWER DELIVERY CONTROLLER HY5515A SPECIFICATION

REVISION 0.4

DOCUMENTATION NUMBER:
DS_HY5515A_R04

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USB Type-C Power Delivery Controller

1 Features

- Support USB PD2.0/3.0/3.2 including programmable power supply (PPS) mode
- Support AVS
- Support UFCS
- Support QC2.0/QC3.0/QC3.0+
- Support SCP/FCP
- Support AFC
- Support PE+1.1/2.0
- Support BC1.2 DCP and Apple2.4A
- Integrated VCONN and support SOP′ for e-marker
- Embedded 16MHz 32-bit ARM MCU
- Embedded 32kB flash and 4kB SRAM
- Built-in 11bit DAC for CV loop and 9bit DAC for CC loop, built-in 10bit ADC
- Integrated Volage (VBUS) regulation, Current sense amplifier, and Constant Current or Constant Voltage mode
- High reliability of DP/DM/CC1/CC2, BV>30V
- HYASIC's unique Zero Power Mode <5mW
- Programmable protections:
  - Output over voltage protection
  - Output under voltage protection
  - CC1/CC2/D+/D- overvoltage protection
  - Overcurrent protection
  - Over Temperature protection
- ESD: ±2kV (DP/DM/CC1/CC2: ±4kV)
- Operating voltage range: 3.3V~32V

2 Applications

- USB PD Quick Chargers
- AC/DC PD Type-C adaptor
- Mobile Chargers

3 Description

HY5515A is embedded a 32-bit MCU with a flash of 32kB, an e-Fuse ROM of 128bits, and a SRAM of 4kB. It is a highly integrated USB Type-C port controller that complies with the latest USB Type-C and PD standards providing cable plug and orientation detection for a single USB type-C connector. Upon cable detection, the HY5515A communicates on the CC wire using the USB PD protocol. HY5515A provides additional functionalities and flexibilities on HYASIC's proprietary technology such as all termination resistors required for a Type-C port, integrated feedback control circuitry for voltage (VBUS) regulation and constant current regulation.

HY5515A is a highly integrated design with few external components. It provides high reliability of the system by integrating various functions and protections.

HY5515A is available with QFN24 package.

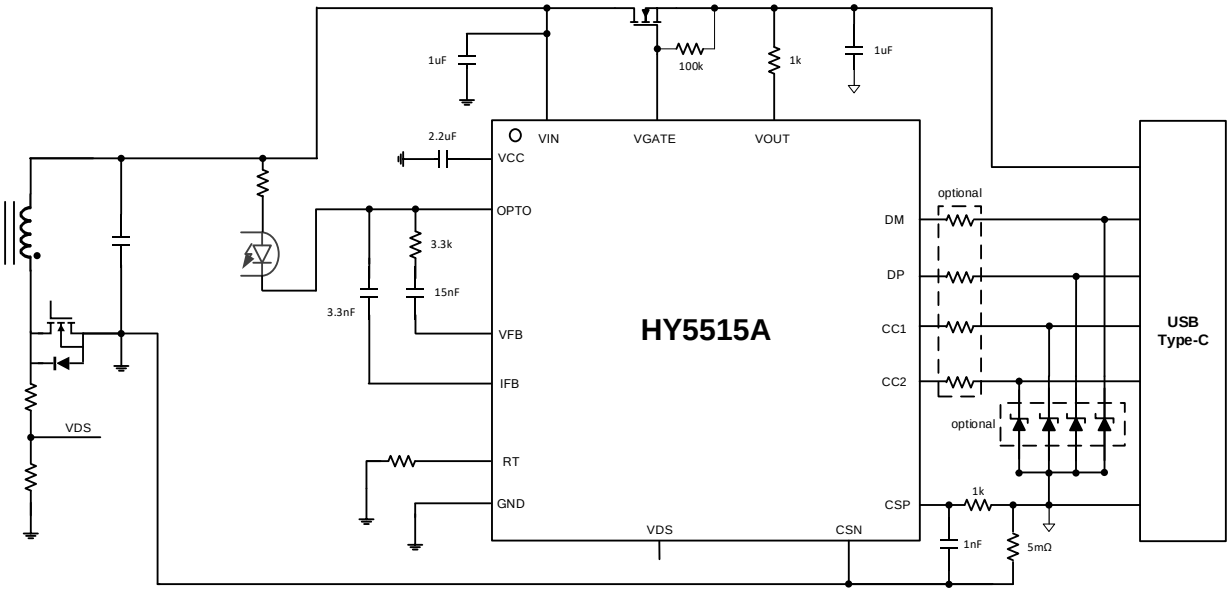
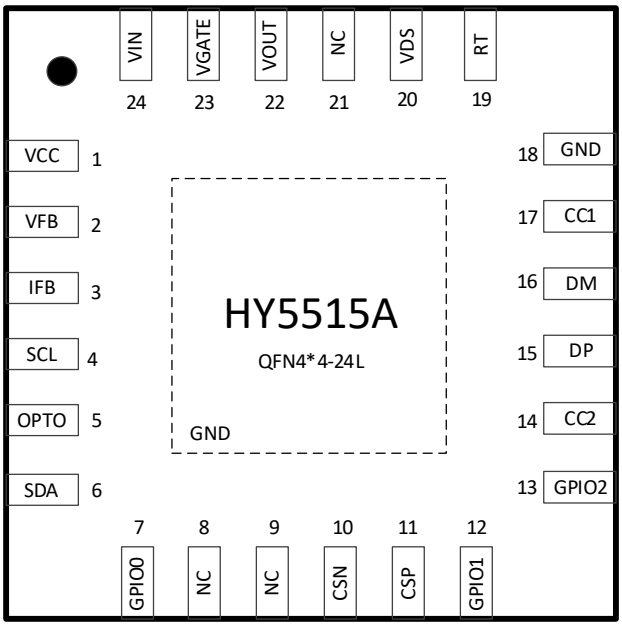


Fig. 1 Typical Single Output PD Application Circuit

4 Pin Configurations and Function Descriptions



QFN-24 (4mm x 4mm)

Fig. 2. Packages Top View

Table 1. Pin Function Descriptions

Pin	Name	Description
1	VCC	Regulated DC bias to supply for the internal circuit. A typical 1uF to 2.2uF X7R bias capacitor is recommended to be designed in applications.
2	VFB	CV loop external compensation pin.
3	IFB	CC loop external compensation pin.
4	SCL	I2C clock line
5	OPTO	Current sink to drive optical coupler. It connects CC loop external component and CV loop external component.
6	SDA	I2C data line
7	GPIO0	general IO
8	NC	Floating, or connect to GND
9	NC	Floating, or connect to GND
10	CSN	CSN pin for sensing resistor input connection, negative signal side
11	CSP	CSP pin for sensing resistor input connection, positive signal side
12	GPIO1	general IO
13	GPIO2	general IO
14	CC2	Configuration channel interface pin 2 to USB Type-C
15	DP	USB positive data line
16	DM	USB negative data line
17	CC1	Configuration channel interface pin 1 to USB Type-C
18	GND	IC ground
19	RT	Connect RT with external NTC. It has internal current source, 100μA(default).
20	VDS	Connect to SR MOSFET drain through resistor divider. It detects a primary side Vbulk voltage. It senses the line voltage and provides the control scheme, protection.

21	NC	Not used, floating
22	VOUT	Output DC voltage bus
23	VGATE	External N-MOSFET gate driver
24	VIN	External DC voltage source input
25	EPAD	IC ground

5 Specification

5.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Unit
VIN, VOUT, DP, DM, CC1, CC2, OPTO, GPIO1, GPIO2	-0.3	34	V
CSN, CSP, GPIO0, VDS, RT, VCC, VFB, IFB, SDA, SCL	-0.3	7	V
VGATE	-0.3	40	V
Operating junction temperature	–40	150	°C
Storage temperature	–40	175	°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

5.2 ESD Ratings

Table 3. ESD Ratings

Item	Description	Value	Unit
Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	DP/DM/CC1/CC2 ±4000	V
		Others ±2000	
	Charged device model (CDM), per JEDEC specification JESD22-C101	±1000	V

5.3 Thermal Specification

Table 4. Thermal Specification

Item	Value	Unit
$R_{\theta JA}$ Junction-to-ambient thermal resistance	90	°C/W
$R_{\theta JC}$(top) Junction-to-case (top) thermal resistance	39	°C/W

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature TJ(MAX), the junction-to-ambient thermal resistance $R_{\theta JA}$, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD(MAX)=(TJ(MAX)-TA)/$R_{\theta JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

5.4 Electrical Characteristics

V_{in} = 5 V, T_{AMB} = 25 °C (unless noted otherwise)

Table 5. Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit
VCC Section							
V_{CC}	VCC voltage					32	V
V_{CC_ON}	VCC UVLO Threshold ON			3			V
V_{CC_HYS}	VCC UVLO Hysteresis				0.4		V
I_{CC_OP}	Normal Operating Current	VCC=5V, VBUS=5V, in normal mode, SR driver is disabled.				7.0	mA
F_{OSC_MCU}	MCU Normal Operation Frequency	In Normal Operation			16		MHz
		In Standby Mode			Disable		MHz
VCC Protection							
V_{CC_OVP}	OVP Threshold. OVP will be disabled during Voltage Transitions	Refer to Target Output Voltage, programable		110		125	%
T_{BL_OVP}	OVP blanking Time	firmware programmable			300		ms
T_{DB_OVP}	OVP Debounce Time	firmware programmable			250		µs
V_{CC_UVP}	Output UVP Threshold	Refer to Target Output Voltage, programable		65		90	%
T_{DB_UVP}	UVP Debounce Time	firmware programmable			1000		µs
T_{BL_UVP}	UVP blanking Time	firmware programmable			300		ms
OCP (Current Through VCC to VBUS)							
I_{OCP}	OCP Current Ratio to Requested Current	Refer to Target Output Current			120		%
T_{OCP_DB}	OCP debounce time	firmware programmable			1		ms
VD+, VD- OVP							
V_{DP_OVP}	DP OVP Threshold	Option 0		4.2	4.35	4.5	V
V_{DM_OVP}	DM OVP Threshold	Option 0		4.2	4.35	4.5	V
$T_{D\_OVP\_deglitch}$	DP, DM OVP Deglitch Time	firmware programmable			200		µs
VDS Section (Line voltage detection)							
V_{LNTH}	Line Voltage Detection Threshold	firmware programmable		0.5		1.2	V
V_{LNTH_HYS}	Line Voltage Detection Threshold Hysteresis				250		mV
Transmitter (CC1, CC2)							
R_{TX}	Output Resistance	During Transmission		33	50	75	Ω
V_{TXH}	Transmit High Voltage			1.05	1.125	1.2	V
V_{TXL}	Transmit Low Voltage			0	37.5	75	mV
T_{BU}	Bit Unit Interval			3.03	3.3	3.70	µs
T_{BMC}	Rising/Falling BMC (Biphase Mark Coding) Time	R_{load}=5.1k, C_{load}=1nF,10% and 90%, minimum is under an unloaded condition.		300		600	ns
Receiver (CC1, CC2)							
V_{RXH}	Receiver HIGH	Rising Edge	00		510		mV
			01		620		
			10		730		
			11		840		
V_{RXL}	Receiver LOW	Falling Edge	00		350		mV

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit
			01		400		
			10		460		
			11		525		
I_{RP_SRC}	CC1/CC2 Broadcasting Current	3A DFP mode	11	304	330	356	uA
		1.5A DFP mode	10	166	180	194	
		Default USB Power	01	64	80	96	
		Disable	00	High Impedance			
V_{OLP_SRC}	Open Loop Voltage for CC1/CC2 Sourcing Current	VCC=5V		2.2	2.8	3.3	V
$V_{CC\_CD\_RD}$	CC1/CC2 Voltage Threshold for Sink Detection	I_{RP_SRC}=330uA	1	2.55	2.60	2.75	V
		I_{RP_SRC}=180uA	0	1.55	1.60	1.75	V
T_{CCDB}	Debounce Time for CC connection	firmware programmable			150		ms
CC1 and CC2 OVP							
V_{CC_OVP}	CC1 and CC2 Over-Voltage Protection Threshold	Option 0		5.5	5.7	5.9	V
$T_{DB\_CC\_OVP}$	CC1 and CC2 Over-Voltage Protection Debounce time	firmware programmable			200		us
CS-Section							
R_{SNS}	Current Sense Resistor				5		mΩ
Voltage Loop DAC Reference							
N_{DAC_CV}	CV DAC Resolution				11		bit
V_{CVDAC_STEP}	CV DAC Voltage Step Including 5V to 32V, 32V to 5V and Soft Start up	Corresponding to 20mV on VOUT			20		mV
Current Loop DAC Reference							
N_{DAC_CC}	CC DAC Resolution				9		bit
V_{CCDAC_STEP}	CC DAC Voltage Step	Corresponding to 20mA on VOUT			20		mA

6 Function Description

6.1 Overview

The HY5515A is a high performance, high integration USB Type-C Power Delivery Controller which is fully compliant with USB Power Delivery Specification Revision 3.2. Besides, The HY5515A also supports BC1.2 DCP, Apple 2.4A, QC2.0/3.0/QC3.0+, UFCS, AFC, FCP, SCP and PE+1.1/2.0 protocols. It is an ideal solution for power supply devices liking car chargers, quick charger adapters, and smart power strips.

HY5515A integrates the CV and CC loop control, cable drop compensation and control scheme inside silicon. A current sampling resistor is connected to a 5Mω alloy resistor on CSN and CSP for current sampling.

HY5515A has multiple protection functions, including output over-voltage protection, D- impedance detection protection, over-current protection and over-temperature protection.

6.2 Function Block

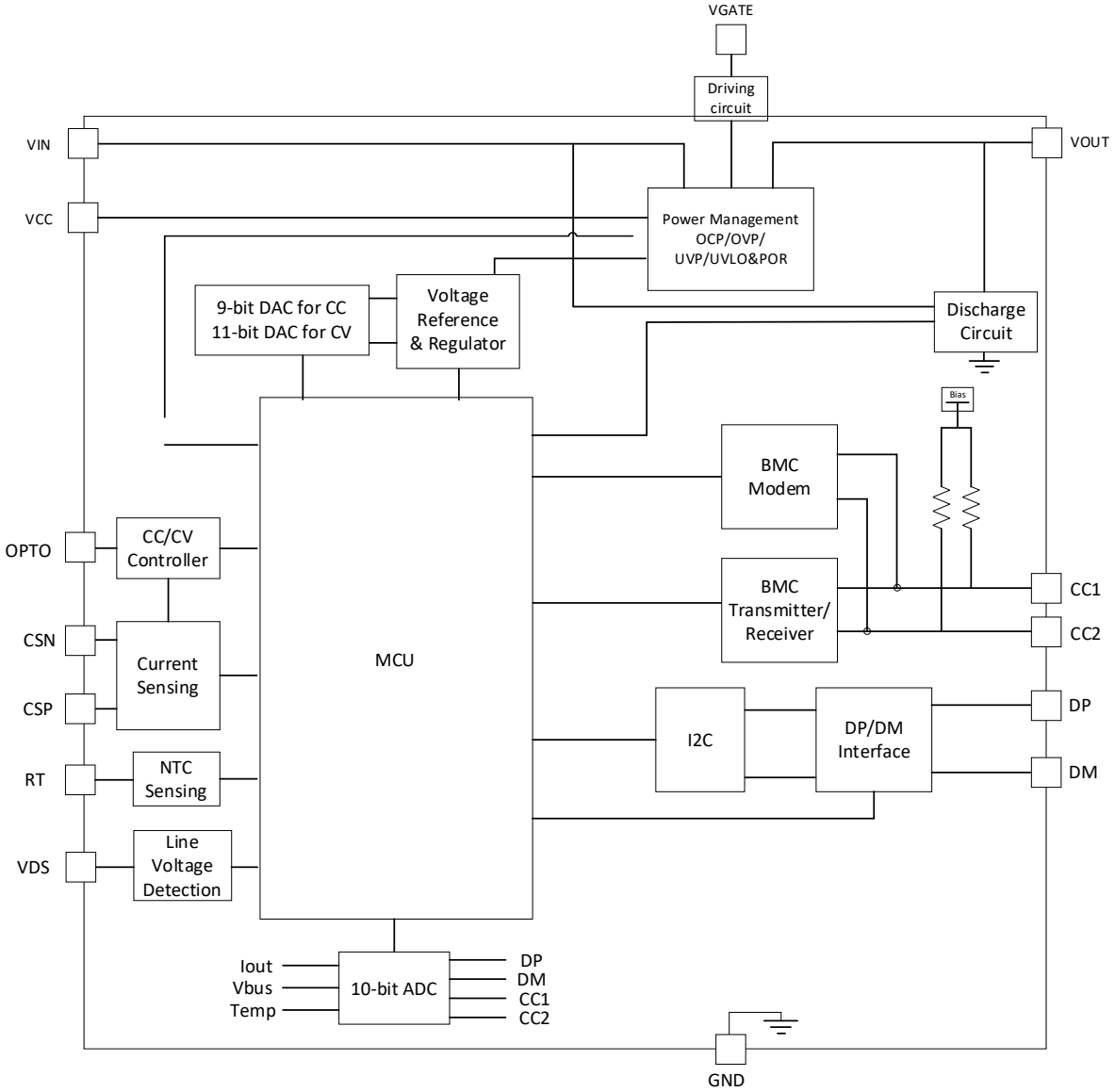


Fig. 3. Function Block

7 Application Notes

7.1 Constant Voltage and Constant Current

CC/CV control scheme implementation is based on error amplifier loop. The simplified block diagram of the CC/CV control is shown as below:

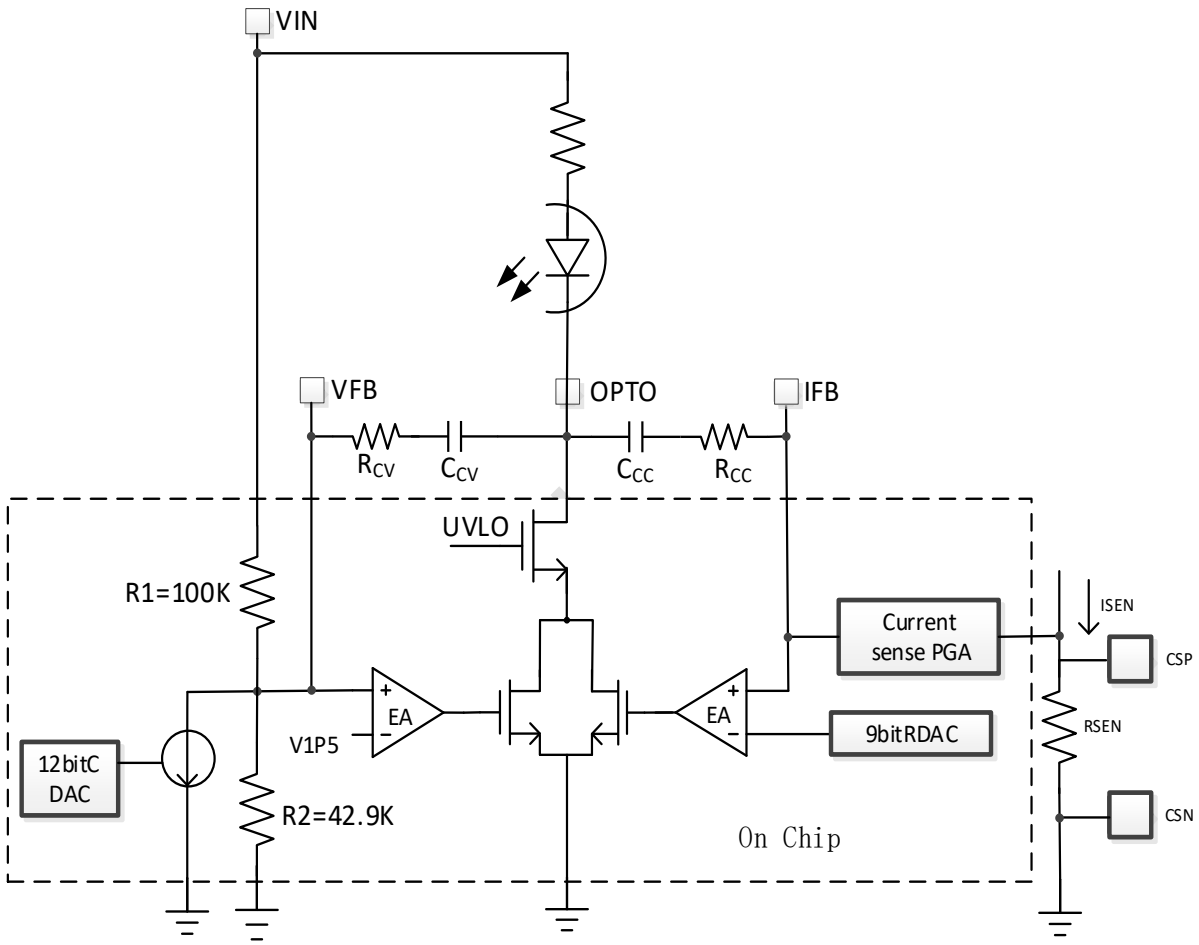


Fig. 4. OPTO Feedback

As shown in the figure below, CV loop control is realized through VFB and OPTO, where OPTO is connected to an external opto-coupler and VFB is connected to a voltage divider network point composed of R1 and R2. VIN voltage can be tuned through 12bit CDAC controlling pulled down current. R1 must be 100K, R2 is 42.9K, which is the value of vout voltage is 5Vunder which the CDAC is off.1LSB CDAC tuning voltage step is 20mv.Full swing is 3v to 32v.

$$\text{Output voltage} = 1.5 * (R1+R2)/R2$$

Equation 1

Constant current control is based on the current sense PGA amplifier the current through CSP and CSN.RSEN can be 5mohm or 10mohm.The constant current can be locked by the EA loop and set by the 9bit RDAC,1LSB is 20Ma.

7.2 Cable Drop Compensation

The Built-in line drop compensation function of HY5515A has programmable compensation coefficient to meet different application, according to output current. HY5515A currently supports five types of line drop compensation coefficients: 0Mv/A, 50Mv/A, 100Mv/A, 150Mv/A, 200Mv/A. The default configuration is 100Mv/A.

7.3 NTC Protection

NTC resistor can be connected by NTC pin in HY5515A. Current source branches of 4Ua,20Ua, 100Ua can be programmable at NTC pin. The NTC flag is the comparator result of the NTC sensing voltage and the temp threshold of 0.28V or 0.4V

7.4 Over Voltage Protection

HY5515A supports OVP by monitoring the voltage of VIN pin, once the voltage exceeds the over voltage threshold of the required the OVP procedure will be triggered, and then HY5515A turns off external NMOS FET quickly.

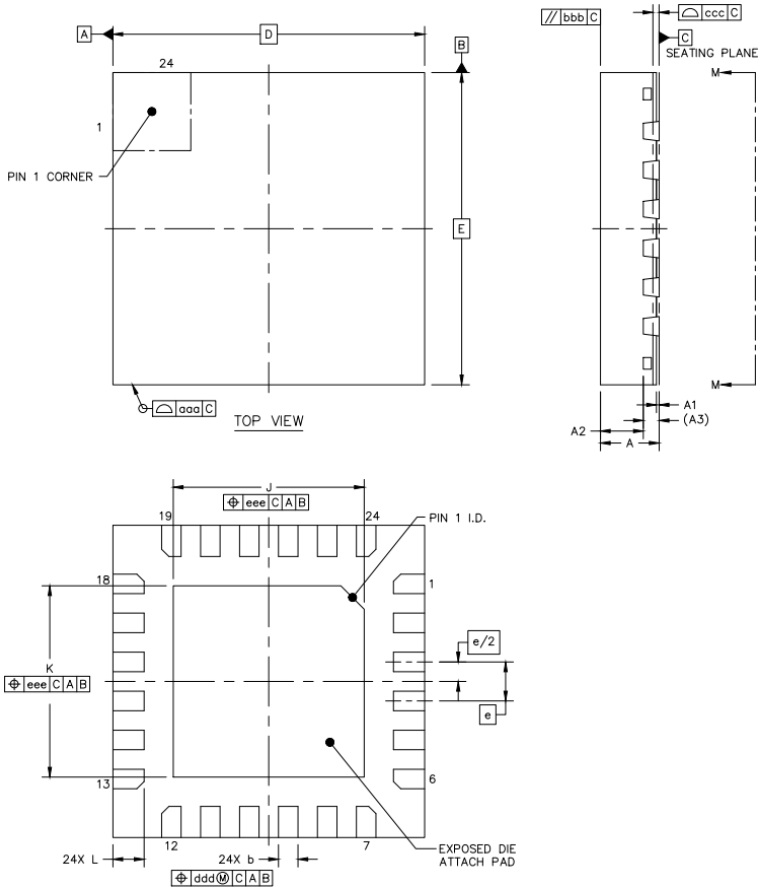
7.5 Over Current Protection and D- Rdm Detection

When the output current exceeds the over current protection threshold or short-circuit protection threshold corresponding to the requested, the over current protection procedure is triggered, and then HY5515A turns off external NMOS FET quickly.

D- RDM detection is applied in AFC application. When the dm RDM detection comparator is alert, the protection procedure is triggered and then HY5515A turns off external NMOS FET quickly.

8 Mechanical, Packaging & Orderable Info

8.1 Package Outline: QFN 4mm x 4mm-24L



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	2.35	2.45	2.55
	Y	K	2.35	2.45	2.55
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

QFN 4mm x 4mm–24L

Fig. 5. Package Outline

8.2 Tape and Reel Information

Package Type	PCs/Reel	Reel/Reel Box	Reel Box/Carton Box	PCs/Carton Box
QFN 4X4-24L	6K	1	5	30K

8.3 Marking and Date Code Information

HY5515A

Product Mark

A BC XX

Year Code Week Code Internal Code

Year		Year Code
2009	2024	A
2010	2025	B
2011	2026	C
2012	2027	D
2013	2028	E
2014	2029	F
2015	2030	G
2016	2031	H
2017	2032	J
2018	2033	K
2019	2034	L
2020	2035	M
2021	2036	N
2022	2037	P
2023	2038	Q

9 Important Notice

10 Contact Information